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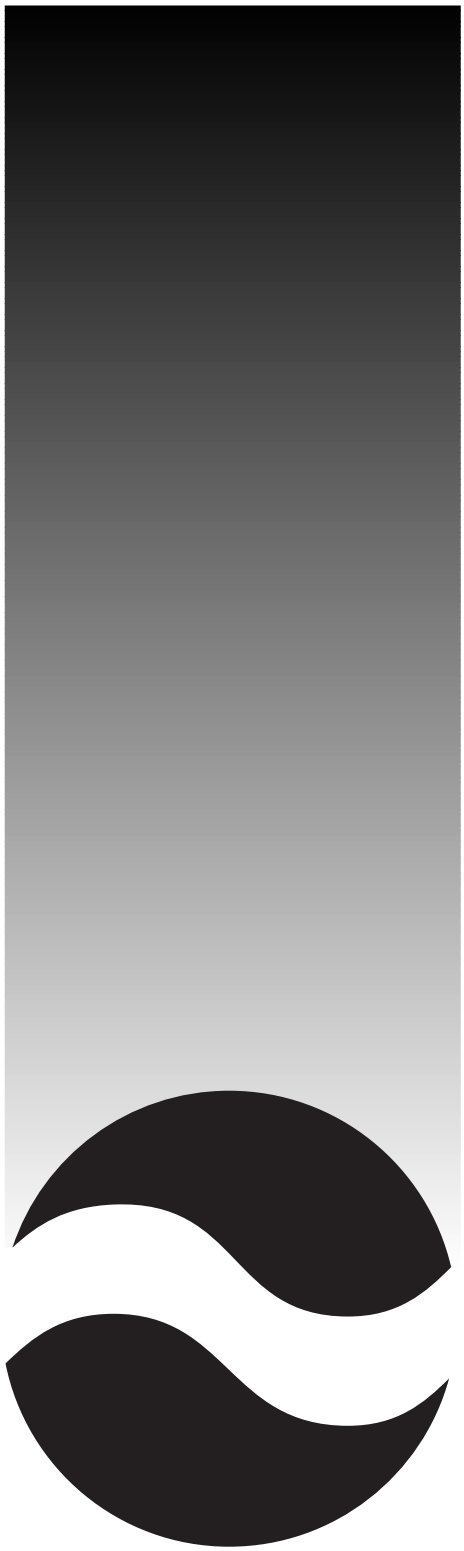
JOINT INDUSTRY STANDARD

Semiconductor Design Standard for Flip Chip Applications



IPC

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IPC/EIA J-STD-026

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About This Document

This document is intended to report on the work being done by several organizations concerned with the design of bare die in flip chip or chip scale configurations. Details were developed by companies who have implemented the processes described herein and have agreed to share their experiences. Readers are encouraged to communicate to the appropriate trade associations or societies any comments or observations regarding details published in this document, or ideas for additional details that would serve the industry.

Users of this standard are encouraged to participate in the development of future revisions.

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Semiconductor Design Standard for Flip Chip Applications

1 SCOPE

This standard addresses semiconductor chip design. It is intended for applications utilizing standard substrates, materials, assembly, and test methods as well as established semiconductor fabrication and bumping processes.

1.1 Purpose The purpose is to provide flip chip design standards which are commensurate with established fabrication, bump, test, assembly, handling and application practices. Addressed are electrical, thermal, and mechanical chip design parameters and methodologies as well as the reliability associated with these items. These standards are intended for new designs as well as modifications of non-flip chip designs.

1.2 Classifications

1.2.1 Bump Process Technologies The following processes for forming bumps on semiconductor die intended for flip chip mounting have proven effective. Some are in full production, others are in development.

(A) Evaporation (tin-lead)

(B) Solder Paste Deposition

(C) Electroplated Tin Lead

(D) Gold Stud Bumping

(E) Conductive Epoxy

(F) Electroless Nickel

Design rules for process technologies A, B and C are well-defined and are detailed in this standard; future revisions will incorporate those rules for the other processes listed as they become available.

1.2.2 Substrate Technologies Four typical mounting structure technologies are listed and affect the design rules of the bare die. These pertain primarily to the precision capability, pitch of bonding site locations, and CTE characteristics.

(W) Organic (Rigid) (see IPC-2222 and IPC-6012)

(X) Flex (Flexible Organic) (see IPC-2223 and IPC-6013)

(Y) Ceramic

(Z) Silicon

1.2.3 Application Classes The reliability of flip chip assemblies will be determined by design decisions. Assumptions are made for each design as to how long it has to survive and in what environment the product will be deployed. In addition, many companies have to determine what is an acceptable failure probability. Table 1 shows the worst case anticipated use thermal environment for nine specific categories. Information is provided on their minimum and maximum temperature excursion, as well as the delta of which the equipment usually sees. Other information provides the details for the cycle time hours, cycles per year, and the years of service expected by the customer. Table 1 also indicates levels of accelerated temperature testing which might correspond to these environments.

Accelerated testing is generally applied in electronics to examine product robustness to anticipated environmental exposures. Common methods include, but should not be limited to, high and low temperature storage, power temperature cycling, thermal cycling/shock and mechanical cycling/shock.

1.2.4 Producibility Level In general, the largest bump pitches are associated with the lowest bump and flip chip assembly process defectivities, the cheapest substrate costs and the most repeatable probe and test results. Tight pitch on the device and substrate lead to high test costs and more complex substrates. Designers should always defer to the largest pitch for manufacturability, consistent with other design goals. Cost tradeoffs should be compared for the substrate and die, (whole system), as the cost can be dominated by either.